Indian J. Phys. 76A (1), 61-63 (2002)

IJP A
— an international journal

Optimisation of drift region width with reference to noise in Si DAR IMPATT diode

J K Mishra, G N Dash[1*], T K Mishra[2] and I P Mishra[1]

Department of Physics, G M College (Autonomous), Sambalpur-768 004, Orissa, India
[1]Department of Physics, Sambalpur University, Jyoti Vihar, Sambalpur-768 019, Orissa, India
[2]Department of Physics, Barpali College, Barpali, Bargarh-768 029, Orissa, India

E-mail : gndash@rediffmail.com

Abstract The noise behaviour of a Si DAR IMPATT diode is studied for different width of the v-region keeping the total diode width constant, using a realistic computer simulation method developed by us. Our results indicate that there exists an optimum width of the drift region of a DAR diode for which the mean square noise voltage of the diode would be the minimum. For a Si DAR diode designed for operation at 80 GHz the optimised width of the v region is found to be 100 nm

Keywords IMPATT, DAR, noise

PACS Nos. 85.30.-z, 73.40.-c, 07.50.Hp

1. Introduction

The idea of Double Avalanche Region (DAR) IMPATT (IMPact ionization and Avalanche Transit Time) diode was first proposed by Som *et al* [1] with a structural form $n^+ p\nu n p^+$, having two avalanche zones around the n^+p and np^+ junctions with a common drift zone in between them. Wide band high frequency analysis of a DAR diode indicates several advantages of this diode for microwave generation [2-4]. The unique feature of DAR diode is the existence of several bands of negative conductance, which may provide multiband-tuning facility. However, it is expected that the existence of two avalanche zones may give rise to more avalanche noise from a DAR diode. The high frequency noise properties of a DAR IMPATT diode, first discussed by Datta *et al* [5], is based on several simplistic assumptions like equal carrier ionisation rates and equal drift velocities for electrons and holes. Since then, no improvement in noise study of DAR diode has been made until recent days. In 1996, Dash, Mishra and Panda were the first [6] to publish a realistic and accurate computer simulation scheme to compute the avalanche noise behaviour of IMPATT and MITATT (Mixed Tunelling Avalanche Transit Time) devices. Subsequently the scheme has been successfully applied to study the noise behaviour of several heterojunction IMPATTs [7,8]. The authors now plan, in this paper, to study the noise behaviour of double avalanche region IMPATT diodes to optimise the ν-region width of the diode in order to realise low noise using the realistic and accurate noise simulation method developed by their group.

2. Method

To study the properties of DAR diode, we have considered a 1-D IMPATT model of $n^+p\nu np^+$ structural form shown in Figure 1. The doping concentration in various regions of the DAR diode is determined by using both the appropriate complementary error function profile in the n^+p and np^+ junction regions and exponential function profiles at the p-ν and ν-n transition regions. The low doped ν-region serves the purpose of drift region. The doping level of ν-region is taken to be slightly more than intrinsic value.

n^+	p	v	n	p^+

Figure 1. Schematic diagram of a DAR diode

The field, current and voltage fluctuations due to noise are considered as small signal in nature. The fluctuations are assumed to constitute shot noise giving rise to a mean square noise current as

$$\left\langle di_c^2 \right\rangle = 2qdfdJ_c A \, , \tag{1}$$

* Corresponding Author

where $dJ_t(x') = q\gamma(x')dx'$ is the current generated due to noise source of $\gamma(x')$ located at x' in the space interval dx', q is the electronic charge, df is the frequency interval and A is the area of the diode. The mean square noise voltage is derived following [6] as

$$<v^2>= 2q^2 df\ A\int |Z_t(x')|^2 \gamma(x')\,dx', \tag{2}$$

where $Z_t(x') = v_t(x')/A\,dJ_t(x')$ is the transfer impedance and $v_t(x') = \int_{x'}^{w} e(x,x')\,dx$ is the terminal voltage produced by noise source $\gamma(x')$. A noise source located at x', generates a noise electric field $e(x,x')$ at every point in the depletion layer of the diode. The noise electric field $e(x,x')$ for a given location of the noise source $\gamma(x')$ is computed by solving the following differential equation

$$\left[D^2 - k^2 + \left(\alpha_n - \alpha_p + 2r_n k\right)D + 2\alpha k - H\right]e(x,x')$$
$$= (1/v\varepsilon)\left[(2qr_p\gamma(x')\right], \tag{3}$$

where

$$H = (2J/v\varepsilon)(\partial\alpha/\partial E) + (\partial/\partial E)(\alpha_p - \alpha_n)(\partial E_m/\partial x),$$
$$v = (v_n v_p)^{1/2},\ k = (1/v)(\partial/\partial t),\ r_n = \left(v_n - v_p\right)/2v,$$
$$r_p = \left(v_n + v_p\right)/2v,\ \alpha = \left(\alpha_n v_n + \alpha_p v_p\right)/2v,\ D = \partial/\partial x.$$

A double iterative computer simulation method developed by our group [6] is used to solve the differential equation for $e(x,x')$ keeping the noise source at the beginning of the generation region. The position of $\gamma(x')$ is then shifted to next space step and the whole process is repeated. The process is continued till $\gamma(x')$ covers the whole generation region. Then the mean square noise voltage is calculated using equation (2). The simulation method is made realistic by incorporating features like mobile space charge, experimentally determined carrier ionisation rates and drift velocities *etc.* [9, 10].

3. Results

For this study, we have considered a Si-based DAR diode of the form $n^+p\nu np^+$. We have chosen the drift region as ν-type whose width is varied from 0 nm to 200 nm keeping the total width constant at 600 nm (300 nm for p-side and 300 nm for n-side including ν-regions are taken to be 1.0×10^{23} m^{-3} and 1.5×10^{23} m^{-3} respectively, while for the ν-region a doping concentration of 1.25×10^{21} m^{-3} is chosen. The operating current density (J) and the diode area (A) are considered to be 2×10^{-8} Am^{-2} and 10^{-10} m^2 respectively. The other simulation parameters are listed in Appendix-A.

The noise behaviour of the Si-based DAR diode with different values of ν-region width are shown in Figure 2. It can be seen from Figure 2 that the mean square noise voltage pe bandwidth *versus* frequency curve shows the general trend o mean square noise voltage for IMPATT diode [6]. It may b mentioned here that the trends in Figure 2 have been supporte by experimental results of Haitz and Voltmer [11]. It is interestin to note from our results shown in Figure 2 that three distinc mean square noise voltage peaks are observed at differen resonant frequencies and the value of mean square noise voltag peak decreases as the resonant frequency increases in eac case. Further, our results indicate that the maximum mean squar noise voltage peak decreases from 1.64×10^{-13} V^{2}s to 5.11 : 10^{-14} V^{2}s as we increase the ν-region width from 0 nm to 100 nr and then increases to 9.13×10^{-14} V^{2}s on further increase c ν-region width to 200 nm (Figure 2). It is worth-mentioning th at the design frequency of 80 GHz, a lowest mean square nois voltage of 3.78×10^{-17} V^{2}s is recorded for the DAR diode havin ν-region width of 100 nm as compared to other structures. Th indicates that DAR diode can generate less noise with a prope choice of ν-region width.

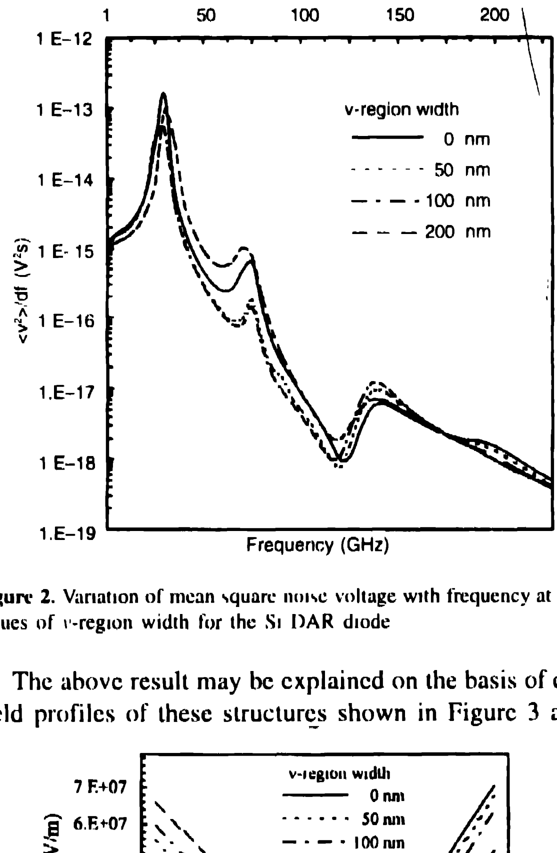

Figure 2. Variation of mean square noise voltage with frequency at differe values of ν-region width for the Si DAR diode

The above result may be explained on the basis of electr field profiles of these structures shown in Figure 3 and tl

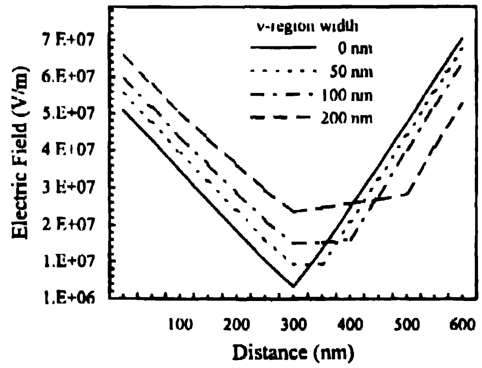

Figure 3. Electric field profiles of the Si DAR diodes with different valu of ν-region width.

ionisation rates of electrons and holes in silicon. Figure 3 shows that for zero ν-region width, the electric field maximum at the n^+p junction is lower as compared to the electric field maximum at the np^+ junction. This indicates that the avalanche zone in p-side is longer as compared to n-side. As the electron ionisation rate is higher than the hole ionisation rate, contribution from p-side to the mean square noise voltage is more as compared to n-side resulting in a sharp peak of mean square noise voltage at resonant frequency. However, it is seen from this figure that when a ν-region is introduced in n-side, the electric field maximum of p-side increases appreciably while that for n-side decreases nominally leading to a narrow avalanche zone in p-side; where as the avalanche zone width in n-side increases nominally. This reduces the carrier ionisation process in p-side, while it remains almost constant in n-side resulting in less noise. This process continues decreasing the mean square noise voltage peak till ν-region width increases up to 100 nm. On further increase of ν-region width, it is observed from Figure 3 that the field maximum increases to a quite higher value in p-side, which results further decrease of avalanche zone width in p-side contributing less noise. On the other hand, the field maximum in n-side decreases to a low value increasing the avalanche region width and hence avalanche noise. In addition to this result it is also observed from this Figure that the strength of electric field in ν-region is enough to constitute avalanche multiplication in this region for 200 nm of ν-region width. Thus the total contribution to mean square noise voltage from ν-region as well as n-side is much higher as compared to p-side for higher ν-region width (200 nm). This results in overall contribution to noise voltage due to the whole diode again high, showing a sharper peak in mean square noise voltage curve for ν-region width of 200 nm. Thus we found that there exists an optimum ν-region width for which the avalanche noise of a DAR diode will be minimum which for the case chosen for this paper is found to be 100 nm.

4. Conclusion

The noise behaviour of Si-based DAR IMPATT diode with $n^+ p\nu n p^+$ structural form has been studied for different ν-region width keeping the total width of the diode constant using a recently developed accurate and realistic computer simulation method. Our results indicate that there exists an optimum value of ν-region width for which the mean square noise voltage is the lowest for a DAR diode. For a Si DAR diode designed for operation at 80 GHz the optimised width of ν-region is found to be 100 nm. A physical reasoning for our findings is also presented considering the electric field profiles of the DAR structures considered in this paper.

References

[1] B Som, B B Pal and S K Roy *Solid State Electronics* **17** 1029 (1974)

[2] D N Datta, S P Pati, J P Banerjee, B B Pal and S K Roy *IEEE Trans. Electron Devices* **ED 29** 1813 (1982)

[3] S P Pati, J P Banerjee and S K Roy *Semicon. Sci. Tech.* **6** 773 (1993)

[4] A K Panda, G N Dash and S P Pati *Semicon. Sci. Tech.* **10** 854 (1995)

[5] D N Datta and B B Pal *Solid State Electronics* **23** 377 (1980)

[6] G N Dash, J K Mishra and A K Panda *Solid State Electronics* **39** 1473 (1996)

[7] J K Mishra, A K Panda and G N Dash *IEEE Trans. Electron Devices* **ED44** 2143 (1997)

[8] J K Mishra, A K Panda and G N Dash *Semicon. Sci. Tech.* **12** 1635 (1997)

[9] C Canali, G Ottaviani and A A Quaranta *J. Phys. Chem. Solids* **32** 1707 (1971)

[10] W N Grant *Solid State Electronics* **16** 1189 (1973)

[11] R H Haitz and F W Voltmer *Appl. Phys. Lett.* **9** 381 (1966)

Apendix–A

The variation of ionisation rates for holes and electrons with electric field can be accounted for using an exponential function of the form

$$\alpha_{n,p} = A_{n,p} \exp(-b_{n,p} / E), \qquad \text{(i)}$$

where the suffix n and p refers to electron and hole respectively and E expresses the electric field. In order to obtain a close fit of equation (i) to the experimental data over the entire field range of measurement, the values of constants $A_{n,p}$ and $b_{n,p}$ are different for different field ranges. Values of these parameters at 200 °C considered for our simulation are listed in Table 1 below.

Table 1. Ionisation rate parameters for electrons and holes in Si

Field range (10^7 Vm^{-1})	A_n (10^8 m^{-1})	b_n (10^8 Vm^{-1})	A_p (10^8 m^{-1})	b_p (10^8 Vm^{-1})
0.0–5.3	0.62	1.31	2.0	2.17
5.3–7.7	0.50	1.22	0.56	1.52

The values of other simulation parameters such as saturated drift velocities ($v_{sn,p}$), mobilities ($\mu_{n,p}$) at 200°C and permitivity (ε) are given in Table 2.

Table 2. Drift velocity and mobility data for electrons and holes in Si alongwith the permittivity data of Si

V_{sn} (10^4 ms^{-1})	V_{sp} (10^4 ms^{-1})	μ_n (10^{-2} m^{2}V^{-1}s^{-1})	μ_p (10^{-2} m^{2}V^{-1}s^{-1})	ε (10^{-10} Fm^{-1})
7.3	6.7	5.8	1.9	1.04